LM64C35P
Passive Matrix Color LCD Unit

FEATURES

- Format: 640 × 480
- Overall Dimensions:
  242.5 (W) × 179.4 (H) × 11.5 (D) mm
- Active Area: 211.2 (W) × 158.4 (H) mm
- Dot Pitch:
  0.085 × RGB (W) × 0.305 (H) mm
- Response/Contrast Ratio: 300 ms/30:1

DESCRIPTION

The LM64C35P is a 640 × 480 dot color display unit consisting of an LCD panel, a Printed Wiring Board (PWB) with electric components mounted onto it, Tape Automated Bonding (TAB) to connect the LCD panel and PWB electrically, and a plastic chassis with CCFT backlight and bezel to fix them mechanically. Signal ground (V_{SS}) is connected with the metal bezel. A DC/DC converter is built in.

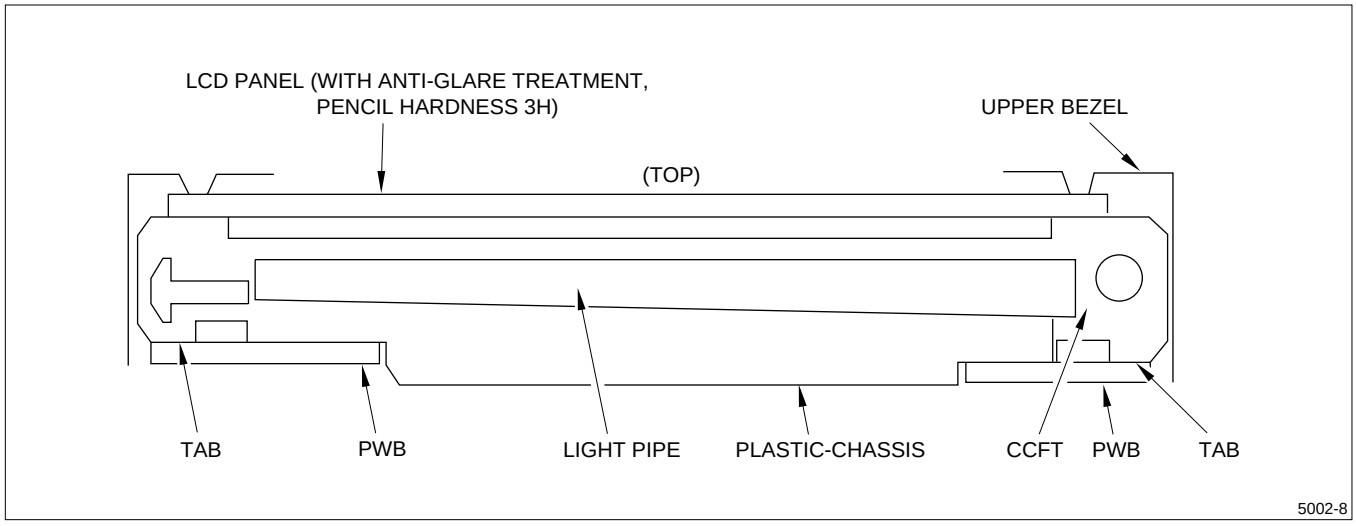


Figure 1. LM64C35P Construction

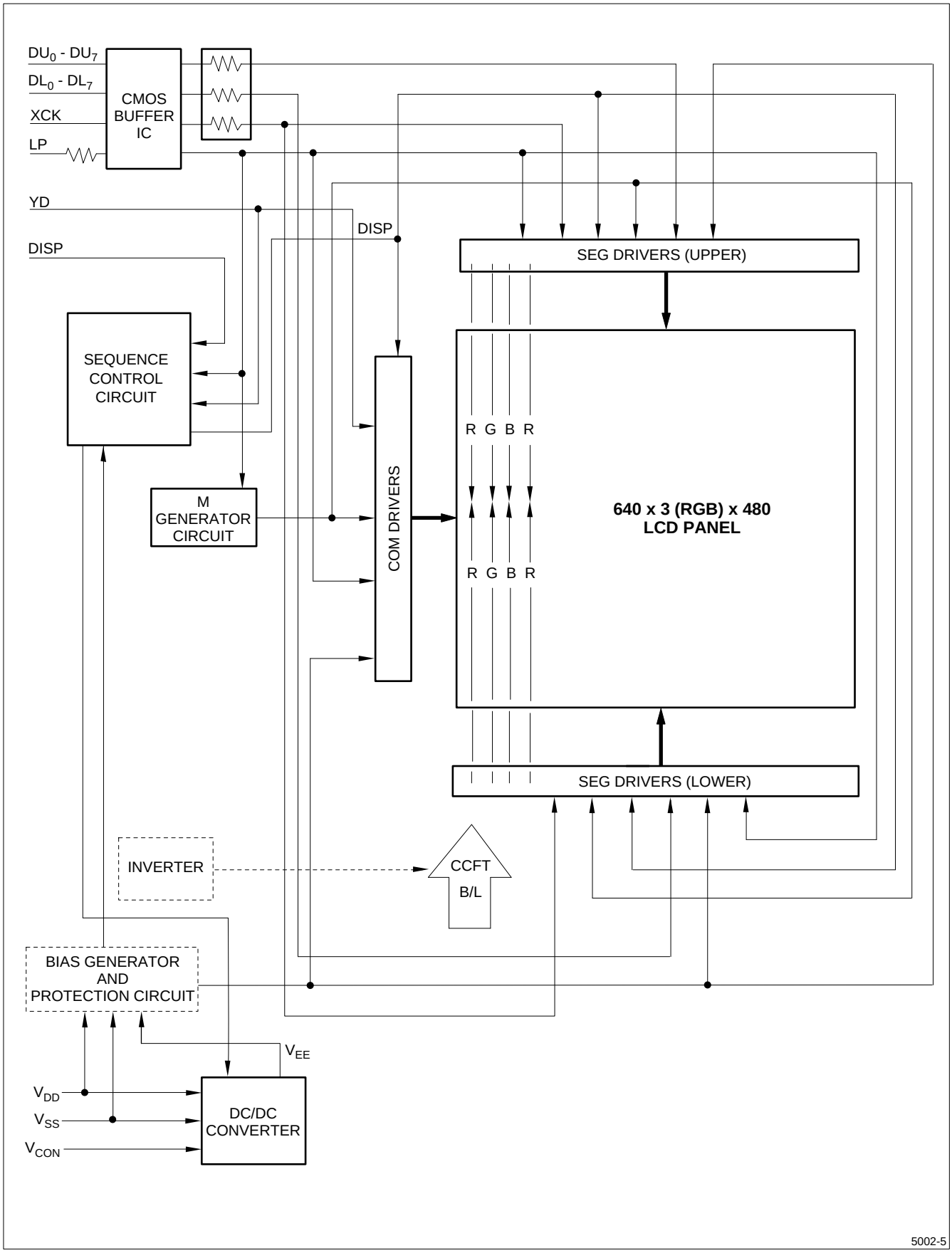


Figure 2. LM64C35P Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT	NOTES
Outline Dimensions	242.5 (W) × 179.4 (H) × 11.5 max (D)	mm	–
Active Area	214.2 (W) × 161.4 (H)	mm	–
Display Format	640 (W) × 480 (H) Full Dots	–	–
Dot Size	0.085 × RGB (W) × 0.305 (H)	mm	–
Dot Spacing	0.025	mm	–
Base Color	Normally Black	–	1, 2
Weight	Approximately 500	g	–

NOTES:

1. Due to the characteristics of the LC material, the colors vary with environmental temperature.
2. Negative-type display:
   Display data 'H': ON → Transmission
   Display data 'L': OFF → Light isolation

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITION
$V_{DD} - V_{SS}$	Supply Voltage (Logic)	0	6.0	V	t_A = 25°C
V_{IN}	Input Voltage	−0.3	V_{DD} + 0.3	V	t_A = 25°C

ENVIRONMENTAL CONDITIONS

ITEM	Tstg		Topr		CONDITION	NOTE
	MIN.	MAX.	MIN.	MAX.		
Ambient Temperature	–25°C	+60°C	0°C	+40°C	–	1
Humidity	–		–		No condensation	2
Vibration	–		–		3 Directions (X/Y/Z)	3
Shock	–		–		6 Directions (±X ±Y ±Z)	4

NOTES:

1. Do not subject the LCD unit to temperatures out of this specification.
2. $t_A \leq 40°C$, 95% RH maximum.
   $t_A > 40°C$, Absolute humidity shall be less than $t_A = 40°C$ at 95% RH.
3. Two hours for each direction of X/Y/Z (six hours as total):

Frequency	10 Hz to 57 Hz	57 Hz to 500 Hz
Vibration Level	–	9.8 m/s^2
Vibration Width	0.075 mm	–
Interval	10 Hz to 500 Hz to 10 Hz/11.0 min.	

4. Acceleration: 490 m/s^2
   Pulse width: 11 ms
   Three times for each direction of ±X/±Y/±Z.

ELECTRICAL CHARACTERISTICS (t_A = 25°C, V_{DD} = 5 V ±10%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTES
$V_{DD} - V_{SS}$	Supply Voltage (Logic)	–	4.5	5.0	5.5	V	1
$V_{CON} - V_{SS}$	Contrast Adjust Voltage	t_A = 0°C	0.8	–	–	V	–
		t_A = 25°C	1.35	1.95	2.55	V	–
		t_A = 40°C	–	–	2.80	–	–
V_{IN}	Input Signal Voltage	'H' Level	0.8 V_{DD}	V_{DD}	VDD +0.3	V	–
		'L' Level	–0.3	V_{SS}	0.2 VDD	V	–
I_{IL}	Input Leakage Current	'H' Level	–	–	1.0	µA	–
		'L' Level	–1.0	–	–	µA	–
I_{DD}	Supply Current (Logic)	–	–	160	240	mA	2
I_{RUSH}	Rush Current (Logic)	t_A = 25°C, Power ON	3 A (pk) × 25 ms + 1 A (pk) × 10 µs (maximum)				
P_D	Power Consumption	–	–	800	1,320	mW	2

NOTES:

1. Under the following conditions:
   a. Immediately after the rise of DISP signal: (3 A × 25 ms)
   b. When the DISP signal is on and kept steady: (1 A × 10 µs)
2. Under the following conditions:
   $V_{CON} - V_{SS}$: Contrast maximum (1.95 V typical), $V_{DD} - V_{SS}$ = 5 V, frame frequency = 73 Hz, display pattern = black/white stripe pattern (Figure 3). This value is direct current.

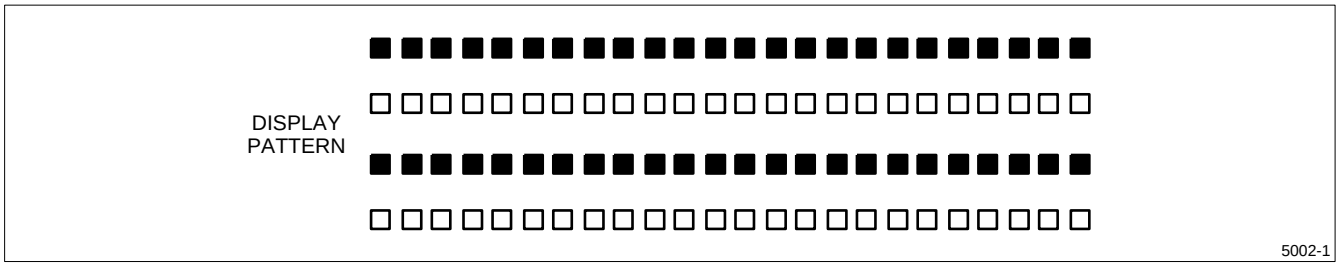


Figure 3. Display High Frequency Pattern

INPUT CAPACITANCE

SIGNAL	INPUT CAPACITANCE (TYPICAL)
YD	20 pF
LP, XCK, DISP	30 pF
DL_0 - DL_7	270 pF
DU_0 - DU_7	270 pF

INTERFACE SIGNALS

LCD [1]

PIN NUMBER [2]	SYMBOL	PARAMETER	LEVEL
1	DL_4	Display Data Signal (Lower)	H (ON), L (OFF)
2	V_{SS}	Ground Potential	–
3	DL_5	Display Data Signal (Lower)	H (ON), L (OFF)
4	YD	Scan Start-Up Signal	'H'
5	DL_6	Display Data Signal (Lower)	H (ON), L (OFF)
6	LP	Input Data Latch Signal	'H' → 'L'
7	DL_7	Display Data Signal (Lower)	H (ON), L (OFF)
8	V_{SS}	Ground Potential	–
9	V_{SS}	Ground Potential	–
10	XCK	Data Input Clock Signal	'H' → 'L'
11	DL_0	Display Data Signal (Lower)	H (ON), L (OFF)
12	V_{CON}	Contrast Adjust Voltage	–
13	DL_1	Display Data Signal (Lower)	H (ON), L (OFF)
14	V_{DD}	Power Supply for Logic and LCD (+5 V)	–
15	V_{SS}	Ground Potential	–
16	V_{DD}	Power Supply for Logic and LCD (+5 V)	–
17	DL_2	Display Data Signal (Lower)	H (ON), L (OFF)
18	DISP	Display Control Signal	H (ON), L (OFF)
19	DL_3	Display Data Signal (Lower)	H (ON), L (OFF)
20	NC	–	–
21	V_{SS}	Ground Potential	–
22	DU_3	Display Data Signal (Upper)	H (ON), L (OFF)
23	DU_4		H (ON), L (OFF)
24	DU_2		H (ON), L (OFF)
25	DU_5		H (ON), L (OFF)
26	DU_1		H (ON), L (OFF)
27	V_{SS}	Ground Potential	–
28	DU_0	Display Data Signal (Upper)	H (ON), L (OFF)
29	DU_6		H (ON), L (OFF)
30	V_{SS}	Ground Potential	–
31	DU_7	Display Data Signal (Upper)	H (ON), L (OFF)

NOTES:

1. Connector used: DF9B-31P-1V (HIROSE)
   Mating connector: DF9B-31S-1V (HIROSE).
2. Pin Number and its locations are shown in the Outline Dimensions diagram.

CCFT [1]

PIN NUMBER [2]	SYMBOL	PARAMETER	LEVEL
1	HV	High Voltage Lineal (From Inverter)	–
2	NC	–	–
3	GND	Ground Line (From Inverter)	–

NOTES:

1. Connector used: BHR-03VS-1 (JST)
   Mating connector: SM03 (4.0) B-BHS or SM02 (8.0) B-BHS (JST)
2. Pin Number and its locations are shown in the Outline Dimensions diagram.

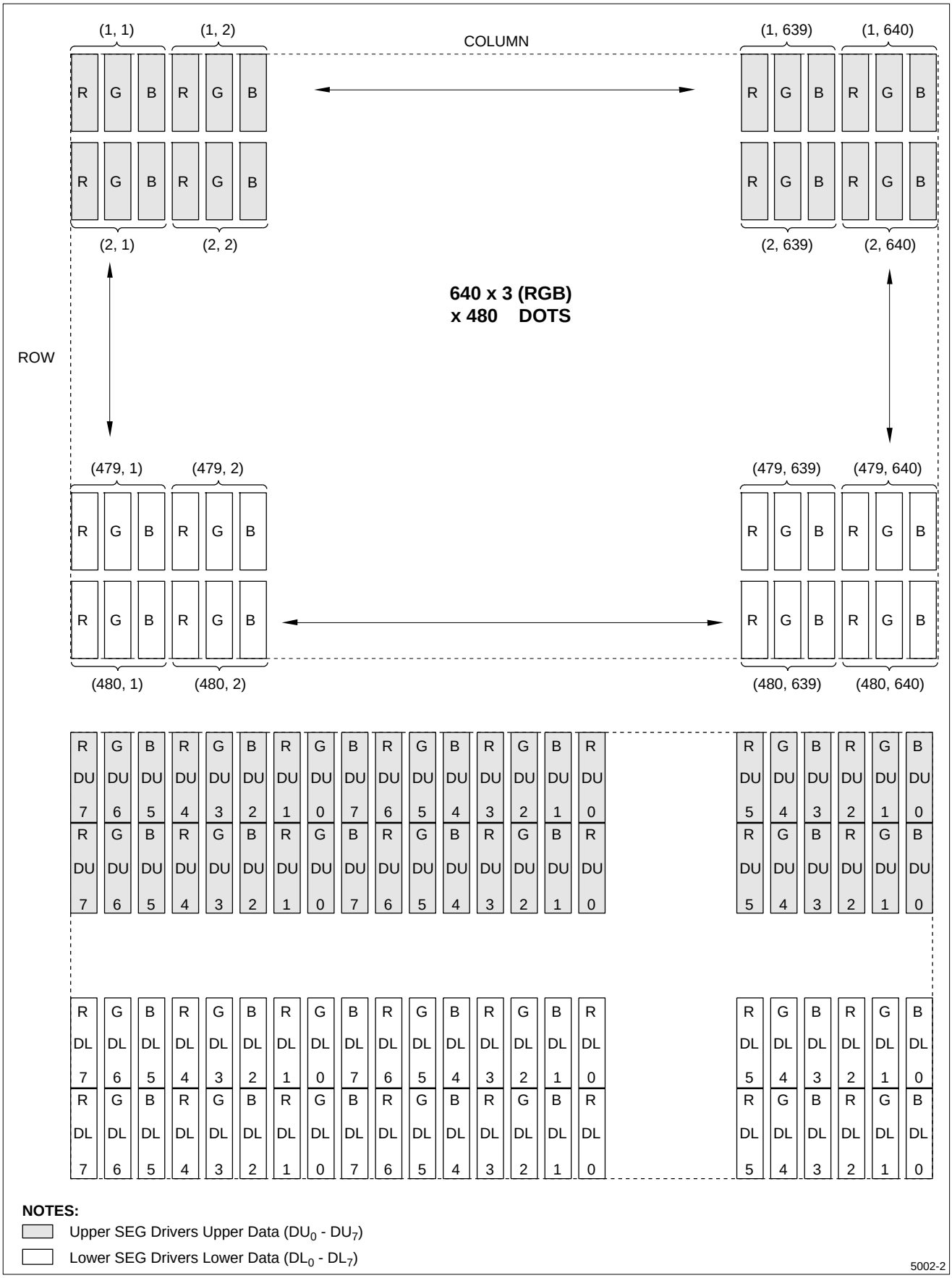


Figure 4. Dot Chart of Display Area

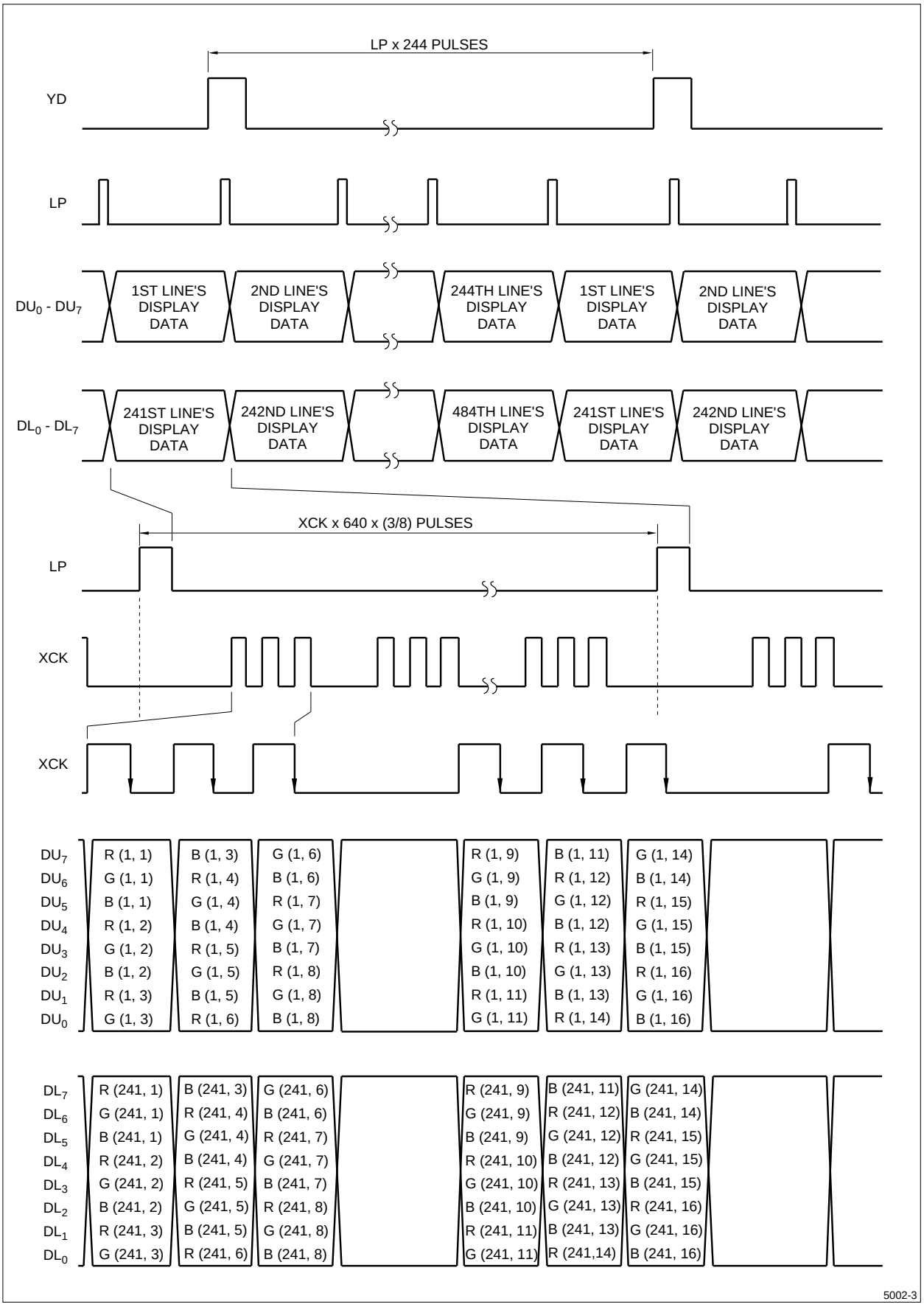


Figure 5. Data Input Timing Chart

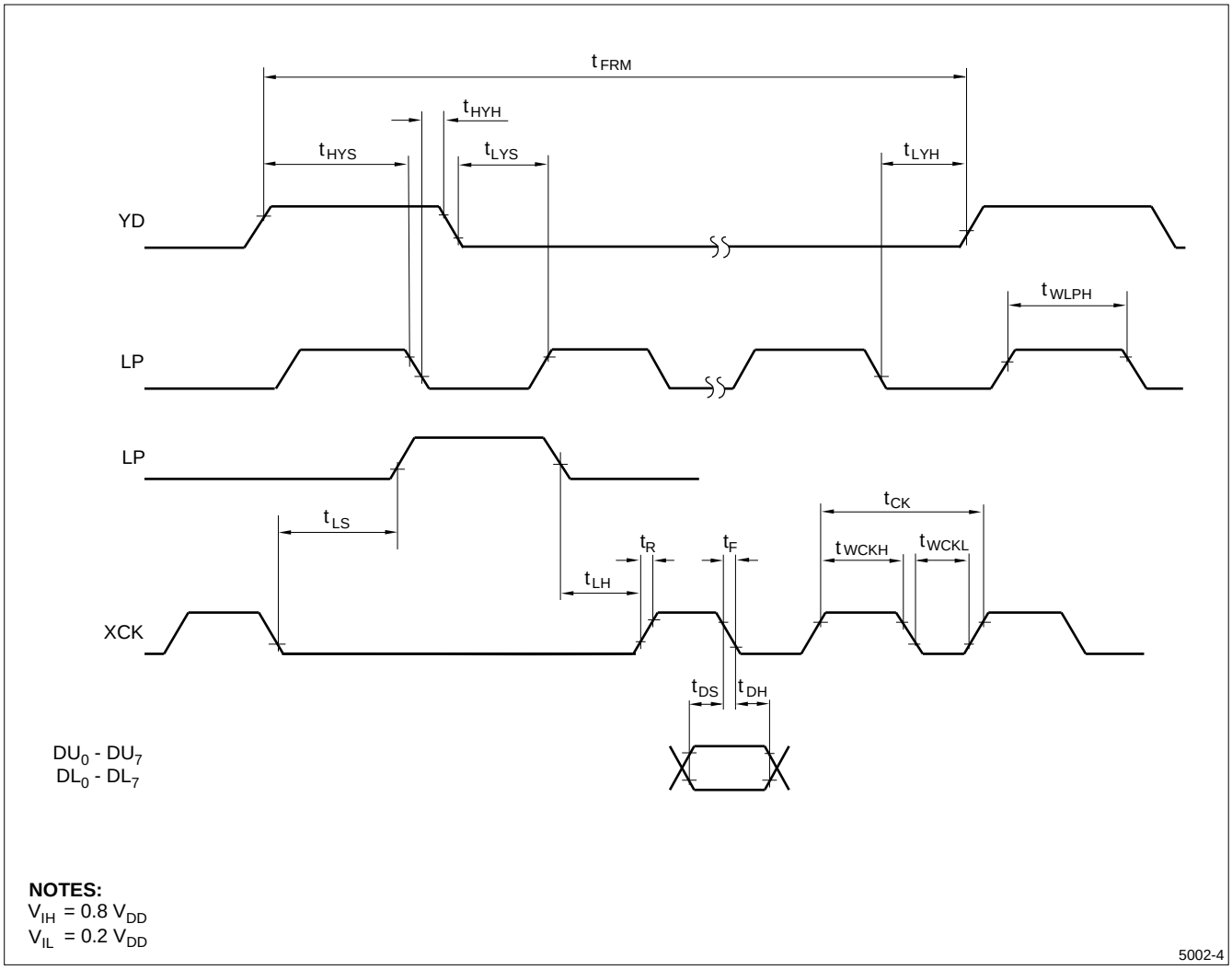


Figure 6. Interface Timing Chart

INTERFACE TIMING RATINGS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTE
t_{FRM}	Frame Cycle	8.33	–	16.94	ms	1
t_{HYS}	YD Signal 'H' Level Setup Time	100	–	–	ns	–
t_{HYH}	YD Signal 'H' Level Hold Time	100	–	–	ns	–
t_{LYS}	YD Signal 'L' Level Setup Time	100	–	–	ns	–
t_{LYH}	YD Signal 'L' Level Hold Time	40	–	–	ns	–
t_{WLPH}	LP Signal 'H' Level Pulse Width	200	–	–	ns	–
t_{CK}	XCK Signal Clock Cycle	82	–	–	ns	–
t_{WCKH}	XCK Signal 'H' Level Clock Width	30	–	–	ns	–
t_{WCKL}	XCK Signal 'L' Level Clock Width	30	–	–	ns	–
t_{DS}	Data Setup Time	30	–	–	ns	–
t_{DH}	Data Hold Time	30	–	–	ns	–
t_{LS}	LP ↑ Allowance Time From XCK ↓	200	–	–	ns	–
t_{LH}	XCK ↑ Allowance Time From LP ↓	200	–	–	ns	–
t_R, t_F	Input Signal Rise/Fall Time	–	–	13	ns	–

NOTE:

1. LCD unit functions at the minimum frame cycle of 8.33 ms (maximum frame frequency of 120 Hz). Due to the characteristics of the LCD unit, 'shadowing' becomes more evident as frame frequency goes up, while flicker is reduced.

   According to our experiments, a minimum frame cycle of 12.8 ms or a maximum frame frequency of 78 Hz demonstrates optimum display quality in terms of flicker and 'shadowing.' Since visual judgment of display quality is subjective and display quality such as 'shadowing' is pattern dependent, decide frame frequency, to which power consumption of the LCD unit is proportional, based on your own thorough testing of the LCD unit with every possible pattern displayed on it.

   The intervals of one LP fall and the next must always be the same, and LPs must be input continuously. The interval must be 70 μs MAX.

UNIT DRIVING METHOD

Circuit Driving Method

Figure 2 shows the block diagram of the unit's circuitry.

Display Face Configuration

The display consists of 640 × 3 (RGB) × 480 dots as shown Figure 4. The interface is a single panel with a double drive to be driven at 1/244 duty ratio.

Input Data and Control Signal

The LCD driver is 160 bits LSI, consisting of shift registers, latch circuits, and LCD driver circuits. Input data for each row (640 × 3 RGB) is sequentially transferred in the form of 8-bit parallel data through shift registers from the top left of the display together with the Clock Signal (XCK).

When input of one row (640 × 3 RGB dots) is completed, the data is latched in the form of parallel data corresponding to the signal electrodes by the falling edge of the Latch Signal (LP). Then, the corresponding drive signals are transmitted to the 640 × 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) is transferred from the scan signal driver to the first row of scan electrodes, and the contents of the data signals are displayed on the first row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of the first row are displayed, the data of the second row are entered. When data for 640 × 3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the second row.

Such data input is repeated up to the 244th row of each display segment, from upper to lower rows, to complete one frame of display using the time-sharing method.

Simultaneously, the same scanning sequence occurs at the lower panel. Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to the LCD panel, causes chemical reaction which deteriorates LCD materials, drive waveform is inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display unit goes up with the clock frequency XCK. To minimize data transfer speed of XCK clock, the driver LSI has a system of transferring 8-bit parallel data through the eight lines of shift registers. This system minimizes power consumption of the display unit.

In this circuit configuration, 8-bit display data is input to data input pins DU_0 - DU_7 and DL_0 - DL_7.

Furthermore, the LCD unit has a bus line system for data input to minimize the power consumption. In this system, data input terminals of each driver LSI are activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

- The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the next right side is selected when data of 160 dots (20 XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.
- This process is followed simultaneously at both the top and bottom column driver's LSIs. Thus, data input is made through the 8-bit bus line sequentially from the left end of the display face.

Since this display unit contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals is shown in Figure 6 and the Interface Timing Ratings table.

OPTICAL CHARACTERISTICS (t_A = 25°C, V_{DD} = 5.0 V, V_{CON} – V_{SS} = Vmax)

The following specifications are based on the electrical measuring conditions, on which the contrast of perpendicular direction (θx = θy = 0°) are maximum.

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT	NOTE
θx	Viewing Angle Range	C_0 > 5.0	θy = 0°	–30	–	30	degrees	1
θy			θx = 0°	–15	–	25		
C_0	Contrast Ratio	θx = θy = 0°		15	30	–	–	2
t_R	Response Time – Rise	θx = θy = 0°		–	220	300	ms	3
t_D	Response Time – Decay	θx = θy = 0°		–	80	100	ms	
x	Unit Chromaticity – White	θx = θy = 0°		–	0.275	–	–	–
y		θx = θy = 0°		–	0.320	–	–	–

NOTES:

1. The viewing angle is defined in Figure 7.
2. Contrast Ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixels 'white' at } V_{MAX}}{\text{Luminance (brightness) all pixels 'dark' at } V_{MAX}}$$

   V_{MAX} is defined in Figure 9.
3. The response characteristics of the photodetector output are measured as shown in Figure 10, assuming that input signals are applied to select and deselect the dots to be measured, in the optical characteristics test method shown in Figure 11.

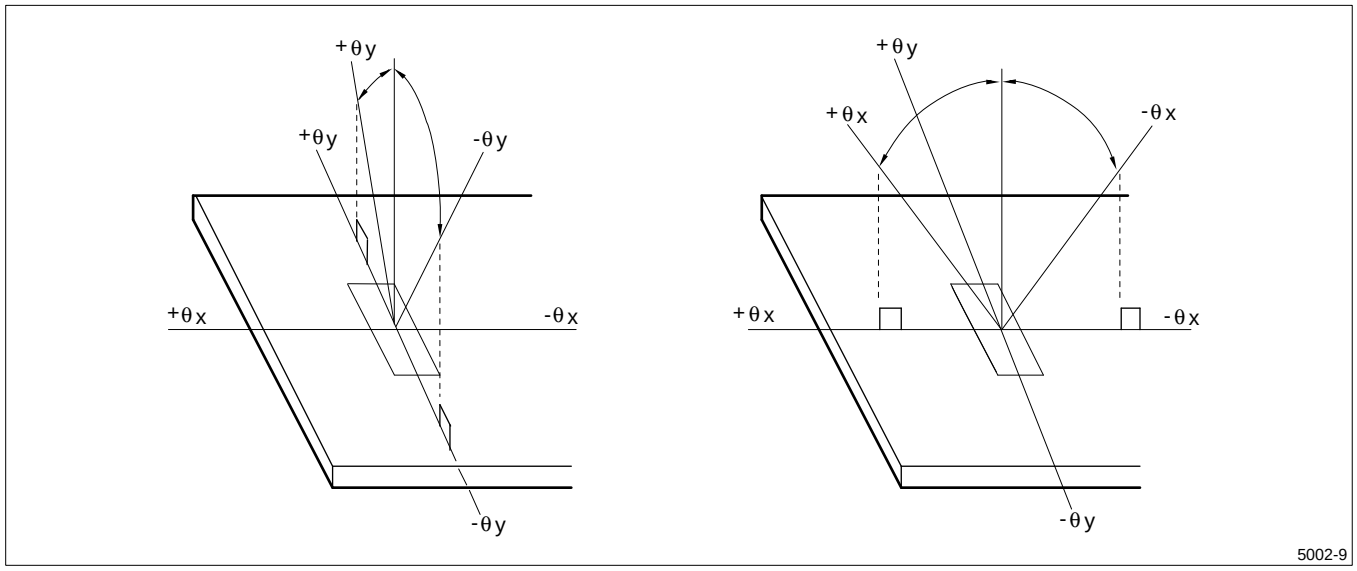


Figure 7. Definition of Viewing Angle

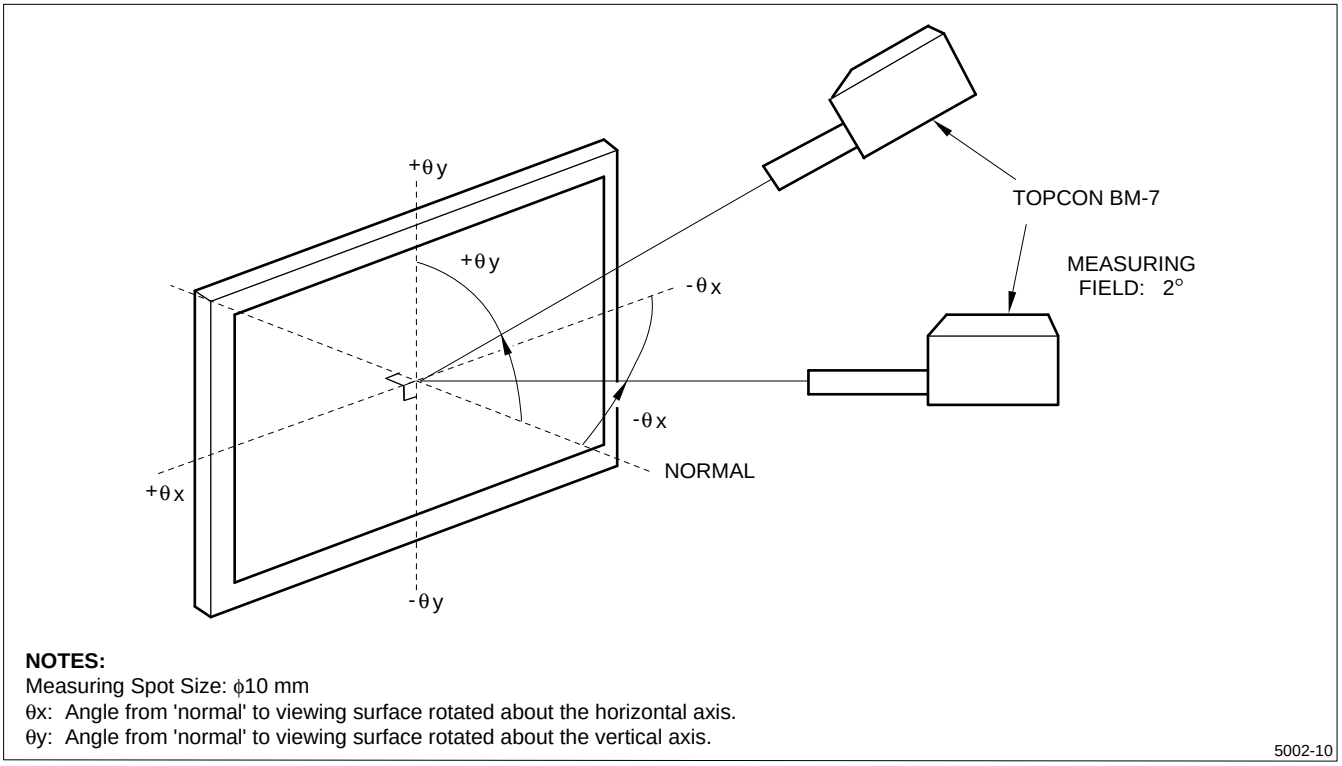


Figure 8. Optical Characteristics Test Method I

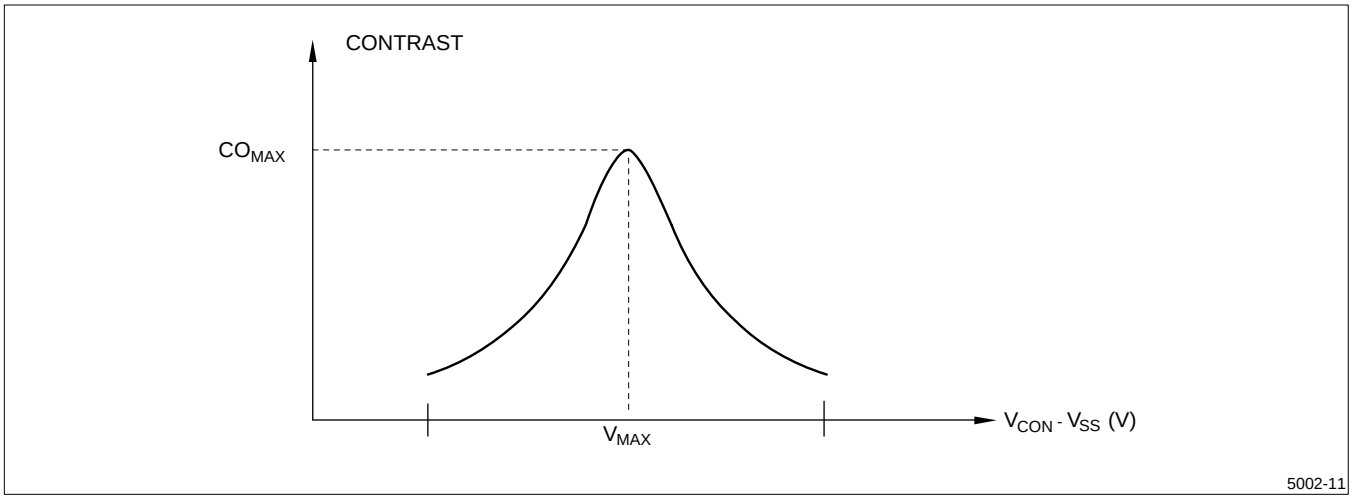


Figure 9. Definition of V_{MAX}

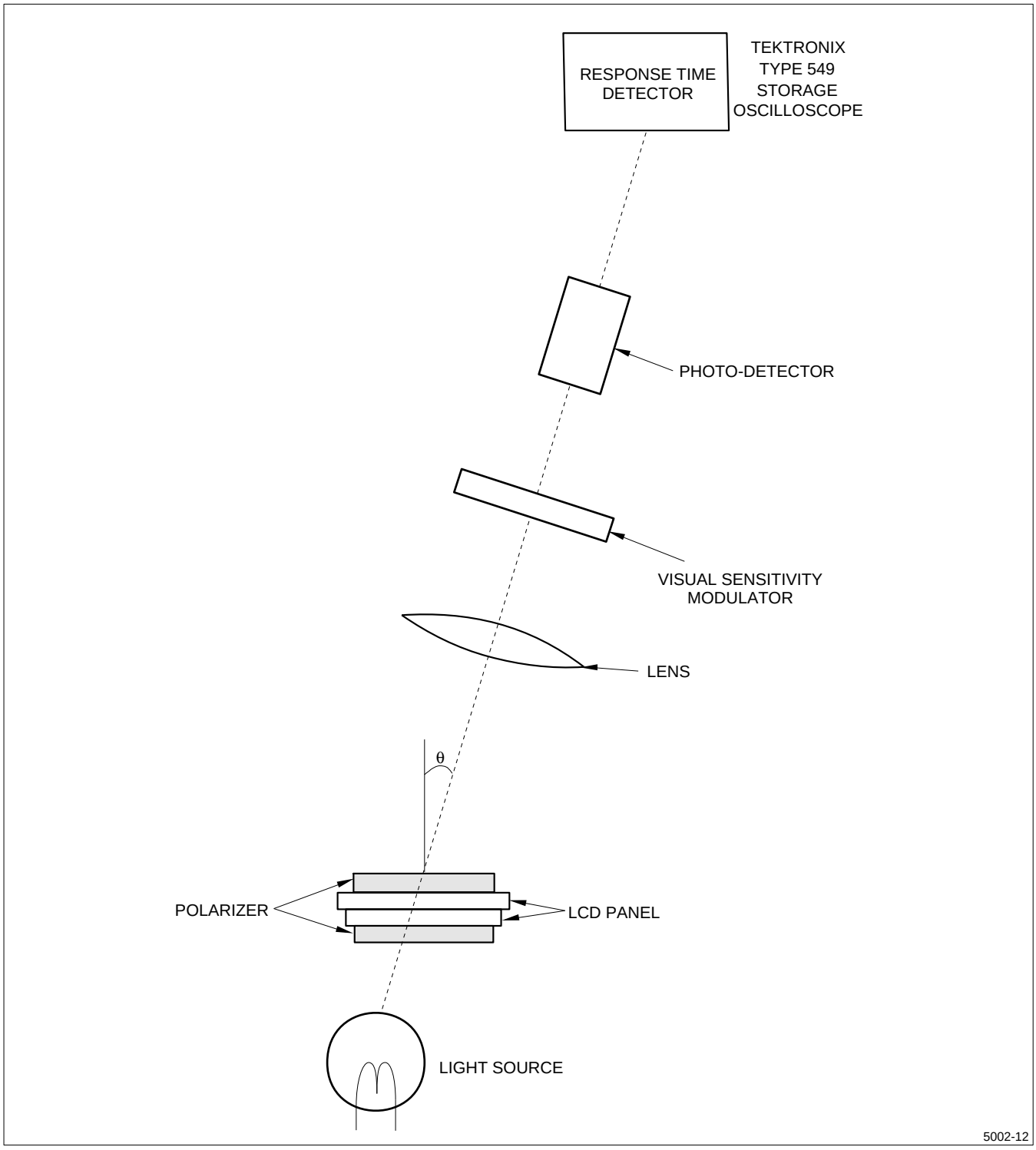


Figure 10. Optical Characteristics Test Method II

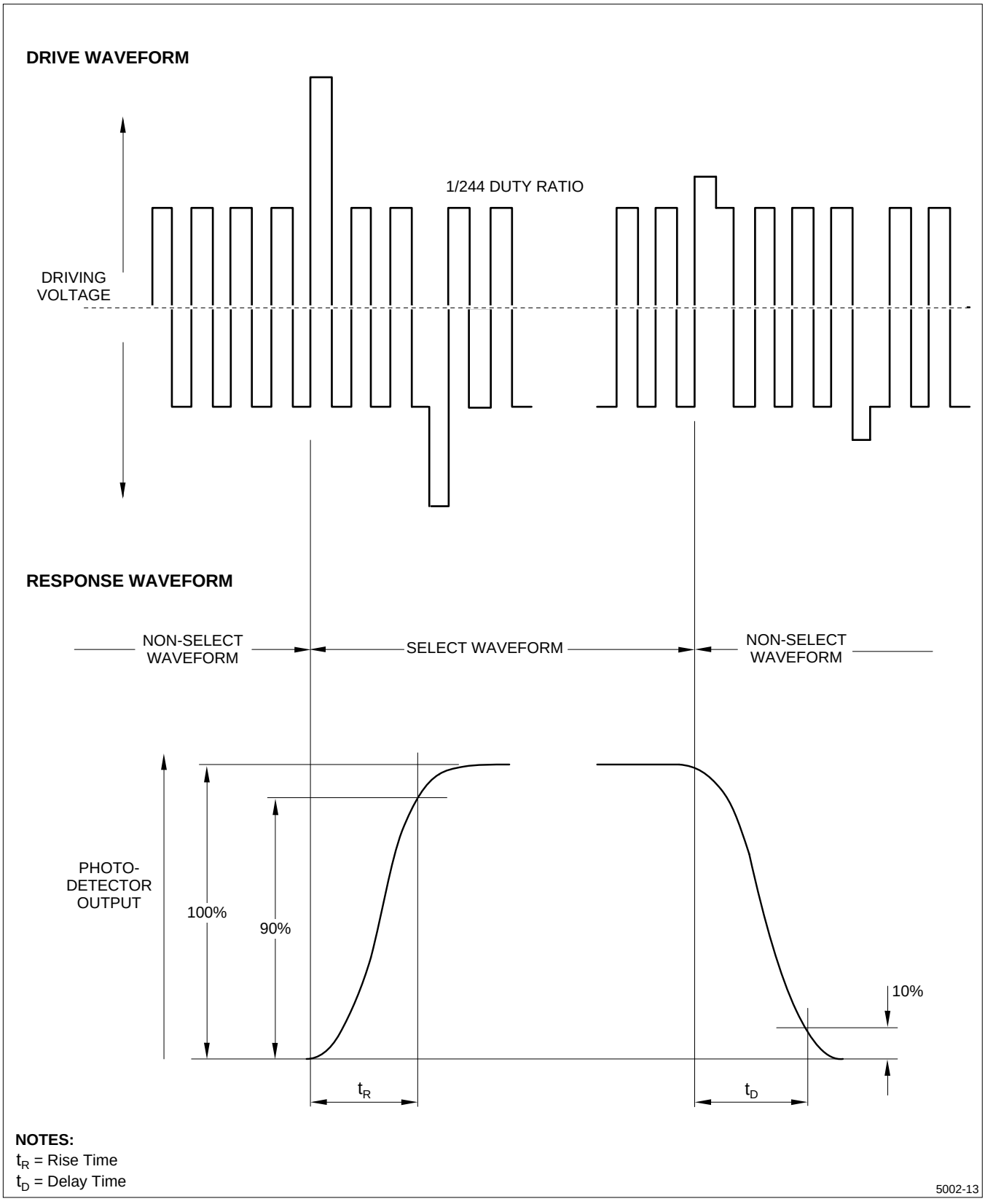


Figure 11. Definition of Response Time

CHARACTERISTICS OF BACKLIGHT

The backlight ratings are provided under the following conditions:

PARAMETER	MIN.	TYP.	MAX.	UNIT
Brightness	50	70	–	cd/m^2

Measurement Circuit

CXA-M10L (TDK) (at IL = 5.4 mA RMS)

Measurement Equipment

BM-7 (TOPCON Corporation)

Measurement Conditions

- Measurement circuit voltage: DC = 9.6 V at primary side.
- LCD: All digits WHITE, V_{DD} = 5 V, $V_{CON} – V_{SS} = V_{MAX}$, DU_0 to DU_7 = 'H' (WHITE), DL_0 to DL_7 = 'H' (WHITE)
- Ambient temperature: 25°C. Measurement taken 30 minutes after turning on the unit.

Lamp Used (Rating, 1 pc.) [1]

HMBS26D10W217C/X Harison Electric Co., Ltd.

PARAMETER		MAXIMUM ALLOWABLE VALUE	NOTE
Circuit Voltage (VS)	480 V_{RMS} (minimum)	–	2
Discharging Tube Current (IL)	5.4 mA_{RMS} (typical)	6 mA_{RMS} (1 pc)	3
Power Consumption (P)	2.6 W	–	4
Discharging Tube Voltage (VL)	1,100 V_{RMS} (minimum)	–	–
Brightness (B)	32,500 cd/m^2 (typical) (1 pc)	–	–

NOTES:

1. Within no conductor closed (CCFT only).
2. The circuit voltage (VS) of the inverter should be designed to have some margin (reference value: 1,450 V RMS minimum), because VS may be increased due to leak current in case of the LCD unit.
3. It is recommended that IL be not more than 5.4 mA RMS so that heat radiation of the CCFT backlight least affects the display quality.
4. Power consumption excludes inverter loss.

Operating Life

The operating lifetime is 10,000 hours or more at 5.4 mA (operating life with CXA-M10L or equivalent).

The inverter should meet the following conditions to keep the specified lifetime of used lamp:

- Sine, symmetric waveform without spike in positive and negative.
- Output frequency range: 25 kHz - 45 kHz.

Allow sufficient burn-in time before executing the operating conditions.

The operating lifetime is defined as having ended when any of the following conditions occur (25 ±1°C):

- When the voltage required for initial discharge has reached 110% of the initial value.
- When the illuminence or quantity of light has decreased to 50% of the initial value.

NOTE: Ratings are defined as the average brightness inside the viewing area specified in Figure 12.

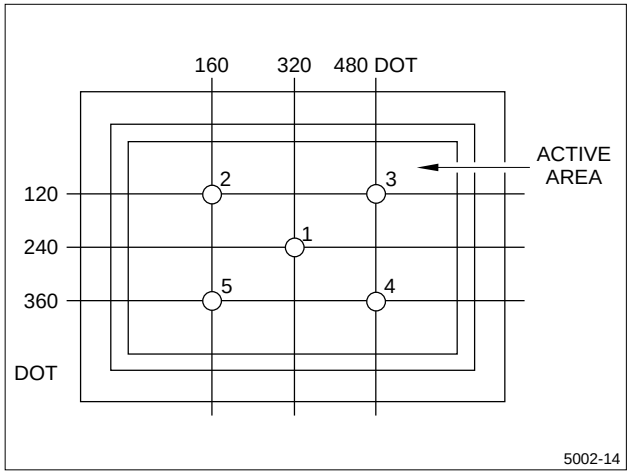


Figure 12. Measuring Points (1-5)

PRECAUTIONS

- Industrial (Mechanical) design of the product in which this LCD unit is incorporated must be made so that the viewing angle characteristics of the LCD are optimized. This unit's viewing angle is illustrated in Figure 13 and as follows:
  - θy MIN < viewing angle < θy MAX
    (For the specific values of θy MIN, θy MAX, refer to the Optical Characteristics table.) Consider the optimum viewing conditions according to the purpose when installing the unit. (Refer to Figure 13.)

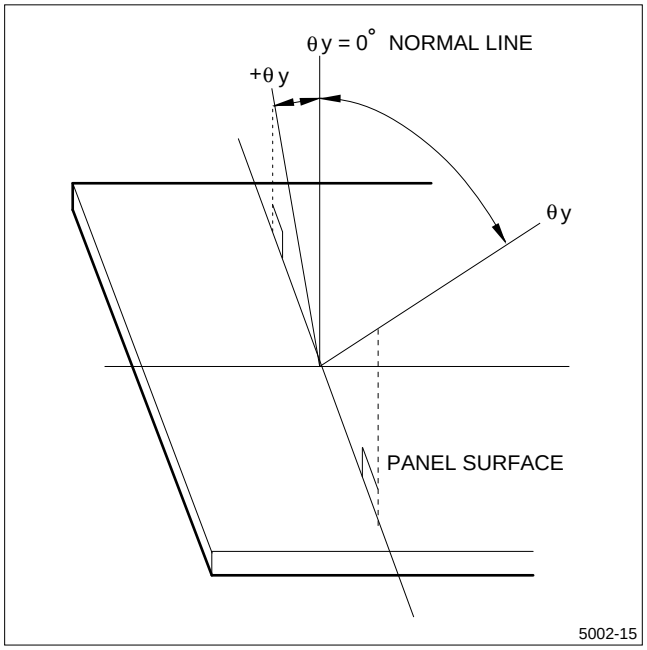


Figure 13. Dot Matrix LCD Viewing Angle

This unit is installed using mounting holes, metal PCB, or bezel. During installation, avoid undue stress on the unit such as twisting or bending. A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.

- Since the front polarizer is easily damaged, use care not to scratch the face.
- If the surface of the LCD cells need cleaning, wipe it with a soft cloth.
- Wipe liquid off immediately since it can cause color changes and staining.
- The LCD is made of glass plates. Use care when handling to avoid breakage.
- CMOS LSIs are equipped in this unit, so care must be taken to avoid electrostatic charge by grounding the human body, etc. Take the following measures to protect the unit from the static electric discharge via mounting tabs from the main system:
  - Ground the metallic case of the main system (contact of the unit and main system).
  - Insulate the unit and main system by attaching insulating washers made of bakelite or nylon.
- The unit should be driven according to the specified ratings to avoid malfunction or permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Avoid latch-up of driver LSIs and application of DC voltage to the LCD panel by following the ON/OFF sequence shown in the 'Supply Voltage Sequence Condition.'
- Since leakage current, which may be caused by routing of CCFT cables, etc., may affect the brightness of the display, the inverter has to be designed taking the leakage current into consideration. Thoroughly evaluate the LCD unit/inverter built into its host equipment to ensure the specified brightness.
- Do not expose the unit to direct sunlight, strong ultraviolet light, etc., for prolonged periods.
- Store the unit at normal room temperature to prevent the LC from converting to liquid (due to excessive temperature changes).
- Do not disassemble the unit.

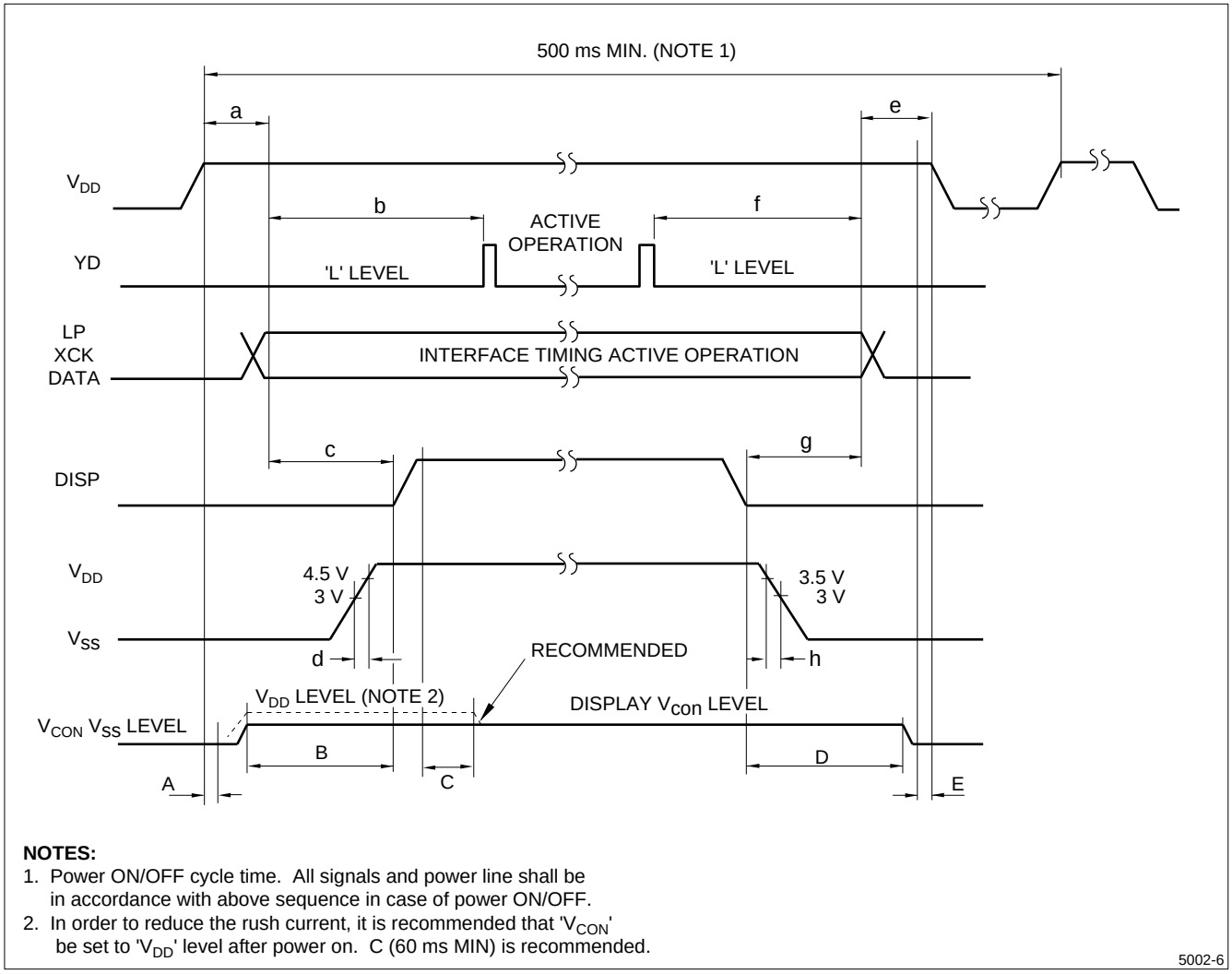
APPLICABLE INSPECTION STANDARD

The LCD unit meets the following inspection standard: S-U-014.

DISPLAY QUALITY

This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, evaluate display quality for the usability of the LCD unit in case gray scale is displayed on the LCD unit.

WARNING: Don't use any materials which emit gas from epoxy resin (Amine's hardener) and silicone adhesive agent (dealcohol or deoxym) to prevent polarizer color change due to gas.



NOTES:
1. Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.
2. In order to reduce the rush current, it is recommended that 'V_{CON}' be set to 'V_{DD}' level after power on. C (60 ms MIN) is recommended.

5002-6

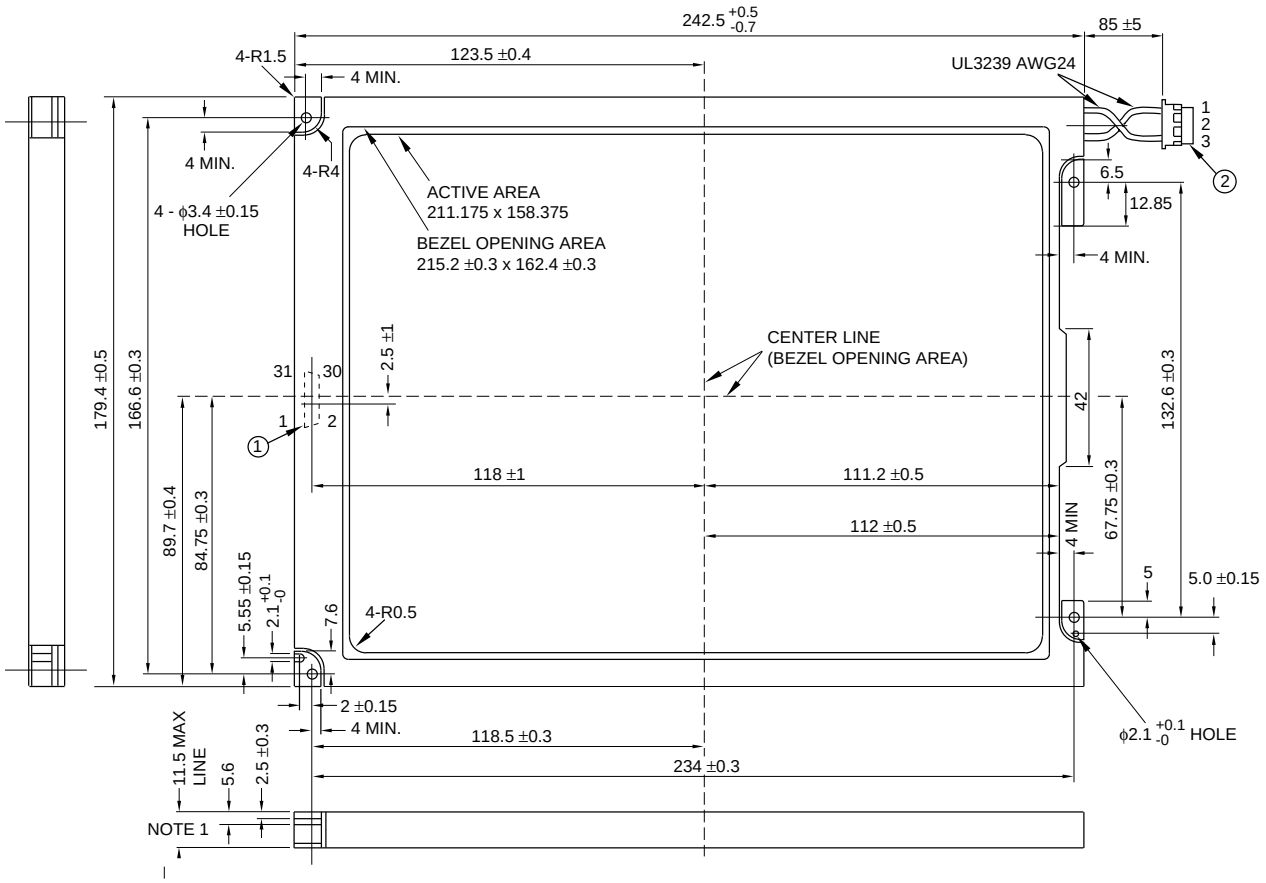
Figure 14. Supply Voltage Sequence Condition

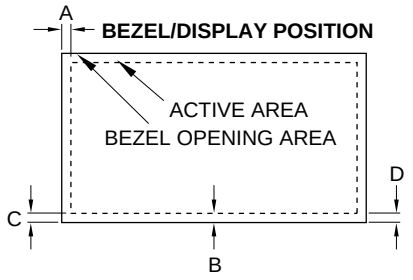
SYMBOL	ALLOWABLE VALUE		NOTE
POWER ON			
a	0 ms (minimum)	1 s (maximum)	–
b	0 ms (minimum)	1 s (maximum)	–
c	LP × 250 (minimum)	1 s (maximum)	–
d	–	25 ms (maximum)	–
A	0 ms (minimum)	–	–
B	0 ms (minimum)	–	–
C	60 ms (minimum) recommended		1

SYMBOL	ALLOWABLE VALUE		NOTE
POWER OFF			
e	0 ms (minimum)	1 s (maximum)	–
f	0 ms (minimum)	–	–
g	0 ms (minimum)	1 s (maximum)	–
h	1 ms (minimum)	–	–
D	0 ms (minimum)	–	–
E	0 ms (minimum)	–	–

NOTE:
1. In order to reduce the rush current, it is recommended that 'V_{CON}' be set to 'V_{DD}' level after power on. C (60 ms MIN) is recommended.

OUTLINE DIMENSIONS





INTERFACE CONNECTOR PIN LAYOUT DF9B-31-P-1V (HIROSE)

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	DL_4	9	GND	17	DL_2	25	DU_5
2	GND	10	XCK	18	DISP	26	DU_1
3	DL_5	11	DL_0	19	DL_3	27	GND
4	YD	12	V_{CON}	20	NC	28	DU_0
5	DL_0	13	DL_1	21	GND	29	DU_6
6	LP	14	V_{DD}	22	DU_3	30	GND
7	DL_7	15	GND	23	DU_4	31	DU_7
8	GND	16	V_{DD}	24	DU_2		

② **CCFT CONNECTOR PIN LAYOUT**
BHR-03VS-1(JST)

PIN #	SYMBOL
1	HDT
2	NC
3	GND

NOTES:
1. Tolerance X-Direction A: 2 ±0.8
2. Tolerance Y-Direction B: 2 ±0.8
3. Obliquity of Display Area: IC-DI < 0.8

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